## Fibonacci sequence with delayed branch

The Fibonacci sequence $F$ is defined as $F(1)=F(2)=1$ and for $n \geq 2$,

$$
F(n+1)=F(n)+F(n-1)
$$

i.e., the $(n+1)$ th value is given by the sum of the $n$th value and the $(n-1)$ th value.

1. Write an assembly program typical of RISC machines for computing the $k$ th value $F(k)$, where $k$ is a natural number greater than 2 loaded from a memory location $M$, and storing the result at memory location $M$.
2. Show the execution of your program on a pipelined processor when $M$ contains the natural number 4. Assume that instructions are fetched from an onboard cache and that there is an instruction window register IW, where one fetched and decoded instruction can be stored. The pipeline stages are F (etch), D (ecode), R (egister read), E(xecute) and W(rite back). Explain where and why delay slots appear.
3. Repeat item 2 , but assume that there is a branch prediction that always gets it right.
4. Repeat item 2 by applying the delayed branch technique.
