Instruction Set Architecture

We present a list of instructions typical of a RISC (reduced set instruction computer) machine. In data-movement and control instructions, the addresses may be immediate $#X$, direct memory $M$, register $r$, or register indirect $(r)$ addresses. Data-processing instructions use immediate or register addressing. PC is the programme counter and $a \leftarrow b$ indicates that the value of $b$ is placed in $a$.

- LOAD $a$, $b$ \hspace{1cm} a \leftarrow b$
- STOR $a$, $b$ \hspace{1cm} a \leftarrow b$
- ADD $a$, $b$, $c$ \hspace{1cm} a \leftarrow b + c$
- SUB $a$, $b$, $c$ \hspace{1cm} a \leftarrow b - c$
- MUL $a$, $b$, $c$ \hspace{1cm} a \leftarrow b \times c$
- DIV $a$, $b$, $c$ \hspace{1cm} a \leftarrow b / c$
- AND $a$, $b$, $c$ \hspace{1cm} a \leftarrow b \& c$
- OR $a$, $b$, $c$ \hspace{1cm} a \leftarrow b \mid c$
- NOT $a$, $b$ \hspace{1cm} a \leftarrow \neg b$
- ASH $a$, $b$, $c$ \hspace{1cm} r \leftarrow b$ (arithmetically) shifted by $c$ positions
- LSH $a$, $b$, $c$ \hspace{1cm} a \leftarrow b$ (logically) shifted by $c$ positions
- BR $a$ \hspace{1cm} PC \leftarrow a$
- BEQ $a$, $b$, $c$ \hspace{1cm} PC \leftarrow a$ if $b$ is equal to $c$
- BNE $a$, $b$, $c$ \hspace{1cm} PC \leftarrow a$ if $b$ is not equal to $c$
- BLT $a$, $b$, $c$ \hspace{1cm} PC \leftarrow a$ if $b$ is less than $c$
- BGT $a$, $b$, $c$ \hspace{1cm} PC \leftarrow a$ if $b$ is greater than $c$
- BLE $a$, $b$, $c$ \hspace{1cm} PC \leftarrow a$ if $b$ is less than or equal to $c$
- BGE $a$, $b$, $c$ \hspace{1cm} PC \leftarrow a$ if $b$ is greater than or equal to $c$

Most instructions have floating-point versions when special floating-point registers are used (but we will not need these).

Most architectures use two addresses, where the first (or second) argument serves both as the target and one of the sources, e.g., ADD $ra$, $rb$ means $ra \leftarrow ra + rb$. For branch instructions BR $X$ means to jump to instruction $X$ (i.e., load the address of instruction $X$ into PC).

We will use a five-stage pipeline: IF (instruction fetch), ID (instruction decode), RR (register read), EX (execute instruction), WB (write back result into register). We will assume that for data-movement instructions the data transfer between the CPU and main memory happens in the execute stage. Note that for some instructions (e.g., LOAD $ra$, $#X$) some of the pipeline stages (e.g., RR) are not needed.
Example

Write an assembly program that computes \(((10 \times 8) + 4) - 7)^2\) and show the delay slots when executed on a five-stage pipeline. Try to minimize the number of registers used. Assume that when an instruction cannot be further processed (e.g., because of some dependency or resource conflict), then it stalls the pipeline.

Here is the code:

\[
\begin{align*}
I1 & \quad \text{LOAD } r1, \ #10 \\
I2 & \quad \text{LOAD } r2, \ #8 \\
I3 & \quad \text{MUL } r1, \ r1, \ r2 \\
I4 & \quad \text{LOAD } r2, \ #4 \\
I5 & \quad \text{ADD } r1, \ r1, \ r2 \\
I6 & \quad \text{LOAD } r2, \ #7 \\
I7 & \quad \text{SUB } r1, \ r1, \ r2 \\
I8 & \quad \text{MUL } r1, \ r1, \ r1
\end{align*}
\]

We make the following assumptions:

1. Instructions are processed strictly in the order they appear in the code.
2. Instructions like \text{LOAD } r1, \ #10 skip the RR and EX stages, and 10 is written into \(r1\) in the WB stage.

Here is the diagram showing delay slots:

|   | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|
| IF| I1| I2| I3| I4| I5| I5| I6| I7| I7| I7| I7| I8| I8| I8| I8| I8| I8 |
| ID| I1| I2| I3| I4| I4| I4| I5| I6| I6| I6| I7| I8| I8| I8| I8| I8| I8 |
| RR|   |   | I3|   | I5|   | I7|   |   |   |   | I8|   |   |   |   |   |
| EX|   |   | I3|   | I5|   | I7|   | I7|   | I7|   | I8|   | I8|   | I8 |
| WB| I1| I2| I3| I4| I5| I6| I7| I7| I7| I7| I7| I8| I8| I8| I8| I8| I8 |

Comments: In cycles 14 and 15, I8 has to wait (\(r1\) is not ready yet).
Alternatively, we can assume that an instruction can jump the queue, provided that this does not alter the outcome of the computation.

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Comments: In cycle 7, I5 has to wait (\(r2\) is not ready yet), in cycle 10, I7 has to wait (\(r2\) is not ready yet).
Exercise

Consider the computation \((M_1 \times M_2) + M_3 - M_4\) where \(M_i\) indicates the content of a memory location. Write an assembly program for the above computation using minimum number of registers. Show the delay slots when the code is executed on a five-stage pipeline.

Assume that there is an internal cache, where fetched and decoded instructions can be stored until they can be further processed.

Comprehensive Exercise

Consider the computation \((M_1 \times M_2) + (M_3 - M_4)\).

1. Write a program in assembly language that performs the above computation. Try to use a minimal number of registers.
2. Draw a diagram showing the execution of your program on a five-stage pipeline using in-order-issue in-order-completion.
3. Identify the dependencies in your code.
4. Draw a diagram showing the execution of your program on a five-stage pipeline using in-order-issue out-of-order-completion.
5. Remove as many dependencies as possible from your code (by using register renaming) and reorder the code to minimize the number of delay slots when executed on a five-stage pipeline. Show the pipeline activity in a diagram.

You can assume that there is an onboard instruction cache from which the instructions are fetched (so there is no resource conflict between fetching an instruction and executing a data-transfer instruction).