Computer Systems Problems – Part 3

1. A nonpipelined processor has a clock rate of 2.5 GHz and an average CPI (cycle per instruction) of 5. An upgrade of the processor introduces a five-stage pipeline. Due to internal pipeline delays the clock rate of the new processor is reduced to 2 GHz. You can ignore penalties due to branch instructions and other delays due to data and register dependencies.

   (a) What is the throughput of the two processors in MIPS (million instruction per second)?

   (b) Try to give a general formula describing the speed-up factor (using the number of pipeline stages and the speed of the CPU's as parameters).

2. A nonpipelined 10 MHz processor has an 'increment memory direct' instruction, which adds 1 to the value in a memory location. The instruction has five stages: fetch opcode (4 cycles), fetch operand address (3 cycles), fetch operand (3 cycles), add 1 to operand (3 cycles), and store operand (3 cycles).

   (a) By what amount (in percentage) will the duration of the instruction increase if we have to insert a bus wait state (i.e., one cycle) in each memory read and memory write operation?

   (b) Assume that an interrupt occurs at the beginning of the fetch operand stage. After how long does the processor enter the interrupt service cycle?

3. Assume a processor uses a two-stage pipeline (fetch–decode and execute) and a 4-byte instruction queue (window). Each instruction is 2 bytes long, and it takes one bus cycle to fetch it. The processor is executing a program in which, on average, every tenth instruction is a jump.

   (a) What fraction of instruction fetch bus cycles is wasted?

   (b) Repeat if the instruction queue is 8 bytes long.

4. Consider the following program:

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I1: Load R1, A
I2: Add R2, R2, R1
I3: Add R3, R3, R4
I4: Mul R4, R4, R5
I5: Add R6, R6, R5
I6: Mul R6, R5, R7
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   (a) What dependencies exist in this program?

   (b) Assume that the above program is executed on a superscalar processor with two fetch units, two decode units, three execution units (one adder, one multiplier and one loader) and two store units. Show the pipeline activity (by drawing a time diagram) using the in-order issue with in-order completion policy.

5. Assume that a 3-stage (fetch-decode, execute, store) pipelined processor skips a fetch-decode stage whenever it has decoded a branch instruction.

   (a) What is the advantage of this policy?

   (b) Assume that a program is executed where, on average, every fifth instruction is a branch. What is the pipeline utilization compared to a program with the same characteristics (e.g., length) but without any branch instructions?