Main Points of the Computer Systems Module

2017–2018

You can find below the topics we have covered during the CS module. Reading the indicated parts of the Stalling books, including the background part [OS, Part One], is essential for a good exam result. Revising the exercises and solving exam questions from previous years are highly recommended as part of the preparation for the exam. See the web page

`http://www.dcs.bbk.ac.uk/~szabolcs/compsys.html`

for more details.

References

[CA] W. Stallings, *Computer Organization and Architecture*, 7th edition or later, Pearson Prentice Hall, 2006.

[OS] W. Stallings, *Operating Systems*, 6th edition or later, Pearson Prentice Hall, 2009.

Computer Architecture

Instruction Sets

[CA, Chapter 10]

- Machine instruction characteristics [CA, Section 10.1]:
  - Elements: operation code, source and result operand references, next instruction reference (often implicit); location of operands: memory, register, I/O device
  - Representation: binary, symbolic (e.g. ADD)
  - Instruction types: data processing (arithmetic and logical), movement (I/O) and storage (memory), program flow control (test and branch)
  - Number of addresses: typically between three and zero; implicit addressing (use of accumulator)
  - Instruction set design: operation repertoire, data types, instruction format (length, no. of addresses), registers (which can be referenced by instructions), addressing modes
- Types of operands [CA, Section 10.2]: addresses: immediate, direct, indirect, displacement, stack; numbers: integer or fixed point, floating point, decimal; characters; logical data
- Types of operations [CA, Section 10.4]:
  - data transfer: move, store, load, set, push, pop
  - arithmetic: add, subtract, multiply, divide
  - logical: and, not, test, shift, rotate
  - I/O: read, write
  - system control: read or alter control register — kernel mode
  - transfer of control: branch, return, skip; procedure call — use of stack
- Assembly language [CA, Section 10.6]

CPU Structure and Function

[CA, Chapter 12]

- Processor organization [CA, Section 12.1]: registers, ALU unit, control unit
- Interconnection structures [CA, Sections 3.3 and 3.4]: bus; control, address and data lines

- Register organization [CA, Section 12.2]:
  - user-visible registers: general purpose, data, address (segment pointers, stack pointer), condition codes/flags (positive, negative, zero, equal)
  - control and status registers: program counter PC, instruction register IR, memory registers MAR and MBR, program status word PSW (flags, interrupts enabled, kernel mode)
- Instruction cycle [CA, Section 12.3]: instruction and data fetch and decode, execute, interrupt; indirect cycle for address calculation; data flow involving registers and bus lines
- Instruction pipelining [CA, Section 12.4]: overlapping the stages of instruction cycles; prefetching instructions
  - timing diagrams, the effect of dependencies and conditional branching; six-stage pipeline (FI, DI, CO, FO, EI, WO);
  - increased complexity of control logic — dealing with branches: loop buffer (high speed memory containing last few instructions), branch prediction (by opcode, dynamically by logging history)
- Overview of Pentium [CA, Section 12.5]: register organization, interrupt processing

Reduced Instruction Set Computers

[CA, Chapter 13]

- Instruction execution characteristics [CA, Section 13.1]: operations (lot of assignments, time-consuming procedure calls), operands (mainly numeric variables)
- RISC characteristics [CA, Section 13.4]:
  - register-to-register operations
  - simple addressing modes
  - simple instruction formats (single size)
  - small set of instructions
- Use of registers:
  - register windows [CA, Section 13.2]: parameter, local and temporary registers, circular organization with overlaps, pointers keep track of active procedures
  - compiler based optimization [CA, Section 13.3]: allocation of physical registers to logical registers, graph coloring according to the active use of registers

- RISC pipelining [CA, Section 13.5]: delayed branch, re-ordering independent instructions (fetch jump before instruction in front of jump — minimizing delay slot)
- Overview of SPARC [CA, Section 13.7]

Instruction-Level Parallelism and Superscalar Processors

[CA, Chapter 14]

- Independent and concurrent execution of instructions in different pipelines [CA, Section 14.1]
- Dependencies [CA, Section 14.1 and 14.2]: true data (write-read), procedural, output (write-write) and antidependencies (read-write), resource conflicts
- Design issues [CA, Section 14.2]: instruction-level and machine parallelisms
  - instruction issue policies (in-order/out-of-order issue, in-order/out-of-order completion)
  - register renaming to remove output and antidependencies
  - branch prediction (static or dynamic — delayed branch is less useful than with RISC)
  - superscalar execution: instruction fetch and branch prediction, re-ordering instructions according to dependencies, execution, committing/retiring instructions (re-order according to program logic); speedup (importance of register renaming)
- Overview of Pentium 4 [CA, Section 14.3]

Operating Systems

Processes and Threads

[OS, Chapters 3 and 4]

Processes

- Definition: program in execution; usage: multiprogramming, pseudo-parallelism; creation; termination; system calls in UNIX and Windows
- States: running, blocked, ready; possible transitions between states; process switch; modes: kernel and user modes, mode switch
- Implementation: process table, process control block

Threads (aka Lightweight Processes)

- Refined process model: resource grouping + thread of execution
- Multithreading: multiple execution in the same process (memory) environment for co-operation by sharing resources
- Modelling threads: multiple threads inside one process; per process data (address space, open files, global variables, etc.) and per thread data (program counter, registers, stack, state, etc.)
- Advantages of multithreading: pseudo-parallelism with shared address space and data, less overhead with switching than with processes, better performance for I/O-bound applications
- Examples: 1) word processor with interactive and background threads, 2) multithreaded web server with dispatcher and worker threads
- Implementations (and their relative advantages):
  - in user space (+: fast context switches, process-specific scheduling algorithms; -: problems with blocking system calls)
  - in kernel (+: easier semantics for blocking system calls; -: costly context switches)
- Microkernels

Scheduling

[CA, Chapter 9]

- When to schedule: process creation and termination, blocking system calls, interrupts
- Goals:
  - general (fairness, policy enforcement, balance)
  - batch systems (throughput, turnaround time)
  - interactive systems (response time)
  - real-time systems (meeting deadlines)
- Preemptive and non-preemptive algorithms
- Scheduling in batch systems:
  - first-come-first-served (FCFS),
  - shortest-job-first (SJF),
  - shortest-remaining-time-next (SRTN)
- Scheduling in interactive systems:
  - round-robin scheduling,
  - priority scheduling (multiple queues),
  - shortest-process-next (aging, weighted average),
- Comparison of the different scheduling algorithms with respect to the scheduling goals; policy versus mechanism
- Thread scheduling: user space and kernel threads
- Scheduling in UNIX and in Windows

Concurrency

[OS, Chapters 5 and 6]

Interprocess Communication

- Race condition between concurrent cooperating processes or threads that share data, examples (spooling directory), consequences
- Critical-section problem; solution should satisfy
  1. mutual exclusion,
  2. no assumption on speed of processes,
  3. progress (no deadlock),
  4. bounded waiting (no starvation)
- Solutions for two processes using busy waiting
  - software: Peterson's solution
  - help from hardware: exchange (swap)
- Semaphores:
  - definition: integer variable with *up* and *down* (or *signal* and *wait*) operations, sleep and wake up, queues
  - usage: eliminates busy waiting, but possible starvation and deadlock
- Monitors (with condition variables)
- Solutions for classical synchronization problems avoiding busy waiting
  - bounded-buffer (producer–consumer)
  - readers–writers
  - dining philosophers
- Interprocess communication (IPC) via message passing as an alternative to shared memory

Deadlock

- Definition: a set of processes is deadlocked if each process in the set is waiting for an event that only another process in the set can cause
- Examples; usually deadlock may occur when processes are granted exclusive access to resources (hardware or software)
- Characterization; the four necessary conditions for deadlock to occur:
  1. mutual exclusion

2. hold and wait
3. no preemption
4. circular wait

- Modelling deadlocks: allocation and request matrices
- Methods for handling deadlocks
  - prevention: deny one of the four conditions above
    mutual exclusion — spooling
    hold and wait — request all required resources initially
    no preemption — take resources away
    circular wait — linearly order resources
  - detection and recovery: detect deadlocks and take recovery action (rollback or kill)
  - avoidance: make sure that the machine reaches only safe states, i.e., that it is guaranteed that there is some scheduling order in which every process can run to completion even if they request their maximum number of resources immediately, Banker's algorithm

Memory Management

[OS, Part Three] Main goal: to allocate (main) memory to processes in an efficient and safe way

- Cache: elements of design (size, write policy, replacement algorithm)
- MM without virtual memory: multiprogramming with partitions
- Virtual memory:
  - provides large logical (virtual) address space for programmers
  - only those parts of the program are in main memory that are currently used by a process
  - mapping between logical and physical addresses
  - paging and segmentation
- Paging:
  - page tables
  - working set and locality of reference, thrashing
- Segmentation: two dimensional address space — virtual memory is divided into logical units (segments); supports protection and sharing

I/O System

[OS, Chapter 11]

- Devices: block and character; communication between device and machine: bus, controller, interrupts
- Programmed I/O, interrupt-driven I/O, direct memory access (DMA)