Problems — 1st batch

1. A CPU is driven by 2 GHz clock.
   (a) Compute the duration of one clock cycle.
   (b) Assume that on average the execution of an instruction takes 4 clock cycles. Compute the performance of the CPU in terms of MIPS (millions of instructions per second).
   (c) Assume that executing a specific program of 400 million instructions takes 2 seconds. How many clock cycles does it take on average to execute an instruction of this program?

2. Consider a machine having 32-bit instructions composed of two fields. The first byte contains the opcode and the remainder an immediate operand or an operand address.
   (a) What is the maximum number of instructions available?
   (b) What is the maximum directly addressable memory capacity (assuming that every address specifies a byte-long word)?
   (c) Discuss the impact on the system speed if the bus has
      i. a 24-bit address bus and a 32-bit data bus, and
      ii. a 16-bit address bus and a 16-bit data bus.
   (d) How many bits are needed for the program counter and the instruction register?

3. Consider a microprocessor, with a 16-bit data bus, driven by an 8 MHz input clock. Assume that this microprocessor has a bus cycle whose duration equals four input clock cycles. What is the maximum data transfer rate across the bus that the microprocessor can sustain in bps (bit per second)? *Hint:* Determine the number of bytes that can be transferred per bus cycle.

4. Consider a 3.2 GHz CPU where executing data processing (arithmetic and logical) instructions takes 4 clock cycles and executing data transfer (load and store) instructions takes 10 clock cycles. When a specific program of one million instructions runs, 60% of the instructions are data processing and 40% of the instructions are data transfer. How long does it take to run this program to completion?

5. When an arithmetic instruction is executed the execution time is

   - 4 clock cycles if the operands can be fetched from the cache
   - 14 clock cycles if the operands have to be fetched from main memory (cache miss).

   The cache hit ratio is 0.6, i.e., 60% of the time the required operands are in the cache. How many clock cycles are needed on average to execute the instruction?

6. A given program needs to read 1 MB data from the hard disk. Data transfer between main memory and the hard disk is done in 1 KB blocks, and it takes 15 ms to read in a block. Determine how much CPU-time is needed for the I/O in case of

   - programmed I/O
   - interrupt-driven I/O
   - using DMA.

   Assume that all the interrupt service procedures needed take 75 ns and you can ignore the initial set-up for the I/O.

   Would it make sense the schedule the given program while the system is waiting for the read to finish?